Yibo Liu

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Ph.D. graduate from VLSI lab, University of California, Riverside. Specializing in machine learning-accelerated optimization techniques for VLSI reliability modeling and design automation. Experience in VLIS methodologies with machine learning applications, fault-tolerant computing, reliability-aware (EM, BTI, HCI, TBBD) design, and management at both the circuit and the system levels. Experience in STA considering OCV and SSTA. Experience in Generative AI models (GAN, VAE, Vision Transformer) and machine learning accelerator design (power, performance, area trade-off).

Technical Skills

- **Programming Languages:** Python, TCL, Shell, Matlab, Verilog, JMP.
- **EDA Skills:** Static Timing Analysis (STA), Spice Simulation, Physical Design.
- **EDA Tools:** Synopsys Tools: PrimeTime, Design Compiler, HSpice, Fusion Compiler; Vivado: HLS.
- **Machine Learning:** PyTorch, Data Mining, Information Retrieval, Recommender Systems. s
- **Data Science:** Information Retrieval | Pandas
- **Embedded Systems:** Scheduling | Linux Kernel | Computer Architecture
- **GPU and Parallel Programming:** CUDA | GPGPU Architecture

Work Experience

Graduate Student Researcher **09/2019 - Present**
VLSI Lab, University of California, Riverside.
Focusing on machine learning accelerated optimization on EDA reliability and design automation.

Technical Intern **06/2022 - 09/2022**
PrimeShield Team, Synopsys Inc.
Assisted the development of a machine learning-accelerated workload-dependent aging-aware STA approach. The new approach counted in the DVFS usage by supporting the scalability of the BTI/HCI aging mission profiles, provided more accurate STA simulation on the actual path, and preventing overly pessimistic aging derates in the current PrimeTime tool to achieve better design PPA.

Education

Ph.D. in Electrical and Computer Engineering **09/2019 - Present**
University of California Riverside, CA, USA

M.S. in Computer Engineering **09/2017 - 06/2019**
University of California Riverside, CA, USA

B.S. in Electrical Engineering **09/2013 - 06/2017**
Huazhong University of Science and Technology, China

Ph.D. Research

Machine Learning (ML)-Accelerated On-chip Power Grid EM-Aware Voltage Failure Fixing

- Utilized Physics Informed Neural Network (PINN) to develop a model for solving partial differential equation based Korhonen equations, enabling efficient Electromigration(EM) stress analysis.
- Applied generative AI models, including generative adversarial networks (GAN), variational autoencoder (VAE) and Vi-Transformer to quickly predict the power grid's EM-aware voltage.
- Modeled EM-aware on-chip power grid fixing scenario as an optimization problem, accelerate the optimization solving process by Machine Learning model acquired sensitivity data (PyTorch AutoGradient) to skip the circuit analysis-based sensitivity calculation.

Improving Device Aging Reliability (TDDB, BTI/HCI) with Approximate Computing (AC) Divider

- Proposed a SOTA approximate stochastic computing divider design that achieves the highest accuracy (close to the theoretical upper limit) and the lowest energy cost among all divider designs.
- Implemented the proposed divider design with Verilog. Functionality test by Synopsys VCS, Synthesis ASIC design with Synopsys Design Compiler.

Improving ML Hardware Accelerator Aging Reliability and Performance with AC Multiplier

- Proposed an approximate stochastic computing multiplier, which can compensate for the delay increase caused by BTI/HCI by reducing the demand computation cycles, and mitigating TDDB-induced errors by including error tolerance encoding.
- Embedded the proposed approximate computing multiplier in the neural network accelerator, which enables the neural network accelerator to trade-off among throughput, accuracy, and power during the inference stage by adjusting the bit-width.
- Started from neural network quantization by PyTorch, and implemented hardware design on Vivado FPGA with C++.

Selected Publications

[J1] Y. Liu, S. Yu, M. Tasnim and X. -D. Tan, **"Fast and Scaled Counting-Based Stochastic Computing Divider Design"**. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024.

[J2] H. Zhou, Y. Liu, W. Jin, Sheldon X.-D. Tan, **"GridNetOpt: Fast Full-Chip EM-Aware IR drop Constrained Power Grid Optimization via Deep Neural Networks"**. IEEE TCAD, 2022.

[J3] Z. Sun, S. Yu, H. Zhou, Y. Liu and S. X. . -D. Tan, **"EMSpice: Physics-Based Electromigration Check Using Coupled Electronic and Stress Simulation"**. IEEE Transactions on Device and Materials Reliability (T-DMR), 2020.

[C1] Y. Liu, and X. -D. Tan, **"GridVAE: Fast Power Grid EM-Aware IR Drop Prediction and Fixing Accelerated by Variational AutoEncoder"**. IEEE/ACM International Symposium on Quality Electronic Design (ISQED), 2024.

[C2] Y. Liu, S. Yu, S. Peng and S. X. -D. Tan **"Runtime Long-Term Reliability Management Using Stochastic Computing in Deep Neural Networks"**. IEEE/ACM ISQED, 2021.

[C3] S. Yu, Y. Liu, Sheldon X.-D. Tan, **"COSAIM: Counter-based Stochastic-behaving Approximate Integer Multiplier for Deep Neural Networks"**. Design Automation Conference (DAC), 2021.

[C4] S. Yu, Y. Liu, Sheldon X.-D. Tan, **"Approximate Divider Design Based on Counting-Based Stochastic Computing Division"**. ACM/IEEE International Symposium on Machine Learning for CAD (MLCAD), 2021.

Teaching

University of California, Riverside

- Teaching Assistant, EE120A Logic Design
- Teaching Assistant, EE168 Introduction to VLSI
- Teaching Assistant, EE213 Computer-Aided Electronic Circuit Simulation